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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/399,919 09/21/99 GINDSAR

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EXAMINER

MAIER, C

ART UNIT

PAPER NUMBER

2675

DATE MAILED:

07/18/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

09/399,919

Applicant(s)

GINOSAR, RAN

Examiner

Christopher J. Maier

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claims ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 September 1999 is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- 15) ☐ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____.
- 18) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other: _____

DETAILED ACTION

Drawings

1. The drawings 1-6 are objected to because the top margins are not acceptable and the lines, numbers and letters are not uniformly thick and well defined, clean, durable and/or black. Correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-4 and 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berger (U.S. Patent No. 4,679,166) in view of Mills (U.S. Patent No. 6,026,465).

As to claims 1 and 8 Berger discloses a plurality of electronic components, including a plurality of input and output devices defining a non-instant on computing device for use in a non-instant on mode of operation in column 1, lines 53-65. Berger further discloses one or more switching mechanisms coupled to the input and output devices and selectively, to selected ones of the first and second plurality of electronic components in column 3, lines 55-68.

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Berger does not disclose an apparatus comprising a first plurality of electronic components defining an instant on computing device for use in a first instant on mode of operation.

Mills discloses an apparatus comprising a first plurality of electronic components defining an instant on computing device for use in a first instant on mode of operation in column 5, lines 56-67.

It would have been obvious to one having ordinary skill in the art at the time of the invention to include Mills' instant on feature with the non-instant on feature of Berger because both Mills and Berger use two processors.

As to claims 2 and 9, Berger discloses that a first plurality of electronic components includes a first processor to execute instructions representing a first operating system in column 1, lines 41-47 and column 2, lines 2-7. Berger discloses that there is a second plurality of electronic components that includes a second processor to execute instructions representing a second operating system in column 1, lines 41-47 and column 2, lines 2-14.

As to claims 3 and 11, Berger discloses that the first plurality of electronic components includes a first memory device and that the second plurality of electronic components includes a second memory device in column 1, lines 41-53. Additionally, Berger discloses that the first and second processors operate simultaneously to synchronize data between the first and second memory devices in figure 1, items 10 and 20, column 1, lines 41-47, and column 3, lines 55-68.

As to claim 4 and 12, Berger discloses that the first or second plurality of electronic components includes a processor having at least two operating modes, wherein when in a first operating mode the processor executes instructions representing a first operating system, and when in a second operating mode the processor executes instruction representing a second operating system in column 2, lines 2-7 and column 3, lines 55-64.

As to claim 10, Berger discloses a connector interface to couple the one or more switching mechanisms to the integrated circuit in column 3, lines 55-68.

3. Claims 5-6 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berger and Mills in view of Stapleton (U.S. Patent No. 6,106,565).

As to Berger and Mills disclosures, see prior rejections.

As to claims 5 and 13, as dependent on claims 1 and 8, respectively, Berger and Mills do not disclose that one or more switching mechanisms includes a mechanical switch.

Stapleton discloses the use of a mechanical switch between two processors in column 6, lines 3-30.

It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the dual processor system of Berger and Mills with the mechanical switch of Stapleton because both deal with dual processors and Stapleton's switch gives the user control over when to make the switch, Stapleton column 6, lines 17-20.

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As to claims 6 and 14, as dependent on claims 1 and 8, respectively, Berger and Mills do not disclose that the mechanical switching means includes a digital multiplexer.

Stapleton discloses that the mechanical switching means includes a digital multiplexer in column 5, lines 63-65.

It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the dual processor system of Berger and Mills with the mechanical switch, including the multiplexer, of Stapleton because both deal with dual processors and Stapleton's switch, which includes the multiplexer, gives the user control over when to make the switch, Stapleton column 6, lines 17-20.

4. Claims 7 and 15, as dependent claims 1 and 8, respectively, are rejected under 35 U.S.C. 103(a) as being unpatentable over Berger and Mills in further view of Jaff (U.S. Patent No. 5,384,692).

As to Berger and Mills' disclosures, see above rejections.

Berger and Mills do not disclose a plurality of input and output devices that include a keyboard and a display device.

Jaff discloses a keyboard and display as input and output devices in figure 3 and column 5, lines 25-37.

It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the dual processor computer system of Berger and Mills with the keyboard and display of Jaff because Jaff is also using a dual

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processor system on his notebook computer system, and keyboards and displays are common input and output devices for computer systems.

5. Claims 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berger and Mills in view of Youens (U.S. Patent No. 6,058,089).

As to claims 1 and 8 Berger discloses a second processor block to operate in a first instant on mode of operation in column 1, lines 53-65. Berger further discloses one or more switching mechanisms coupled to the input and output devices and selectively, to selected ones of the first and second plurality of electronic components in column 3, lines 55-68.

Berger does not disclose a first processor block to operate in a first instant on mode of operation.

Mills discloses an apparatus comprising a first plurality of electronic components defining an instant on computing device for use in a first instant on mode of operation in column 5, lines 56-67.

It would have been obvious to one having ordinary skill in the art at the time of the invention to include Mills' instant on feature with the non-instant on feature of Berger because both Mills and Berger use two processors.

Berger and Mills do not disclose that data can from the first and second processors can be sent to a plurality of external devices.

Youens discloses the connection of an external peripheral device to a notebook computer in figure 1 and column 1, lines 27-38 and 61-67.

It would have been obvious to one having ordinary skill in the art at the time of the invention to include the external drive connection of Youens with the two processor system of Berger and Mills because all deal with compact computers, with one of the design goals being that the computer is small in size and easily transportable, allowing some parts of computers to be connected externally and removed when not necessary, as certain devices are not essential to the computer at all times, Youens column 1, lines 33-37.

6. Claims 17, with respect to claim 16, is rejected under 35 U.S.C. 103(a) as being unpatentable over Berger, Mills and Youens, in further view of Jaff (U.S. Patent No. 5,384,692).

As to Berger, Mills and Youens', disclosures, see above rejections.

Berger, Mills and Youens do not disclose a plurality of input and output devices that include a keyboard and a display device.

Jaff discloses a keyboard and display as input and output devices in figure 3 and column 5, lines 25-37.

It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the dual processor computer system of Berger and Mills with the keyboard and display of Jaff because Jaff is also using a dual processor system on his notebook computer system, and keyboards and displays are common input and output devices for computer systems.

As to claim 18, Berger discloses that the first plurality of electronic components includes a first memory device and that the second plurality of electronic components includes a second memory device in column 1, lines 41-

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53. Additionally, Berger discloses that the first and second processors operate simultaneously to synchronize data between the first and second memory devices in figure 1, items 10 and 20, column 1, lines 41-47, and column 3, lines 55-68.

7. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berger and Mills in view of Stapleton (U.S. Patent No. 6,106,565).

As to Berger, Mills, and Youens', disclosures, see prior rejections.

As to claim 19, as dependent on claim 16, Berger and Mills do not disclose that one or more switching mechanisms includes a mechanical switch.

Stapleton discloses the use of a mechanical switch between two processors in column 6, lines 3-30.

It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the dual processor system of Berger and Mills with the mechanical switch of Stapleton because both deal with dual processors and Stapleton's switch gives the user control over when to make the switch, Stapleton column 6, lines 17-20.

As to claim 20, as dependent on claims 16, Berger and Mills do not disclose that the mechanical switching means includes a digital multiplexer.

Stapleton discloses that the mechanical switching means includes a digital multiplexer in column 5, lines 63-65.

It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the dual processor system of Berger and Mills with the mechanical switch, including the multiplexer, of Stapleton because both deal with

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dual processors and Stapleton's switch, which includes the multiplexer, gives the user control over when to make the switch, Stapleton column 6, lines 17-20.

7. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Berger in view of Mills.

Berger discloses a memory device with a plurality of memory banks in column 1, lines 41-53. Berger discloses that a first plurality of electronic components includes a first processor to execute instructions representing a first operating system in column 1, lines 41-47 and column 2, lines 2-7. Berger discloses that there is a second plurality of electronic components that includes a second processor to execute instructions representing a second operating system in column 1, lines 41-47 and column 2, lines 2-14. Berger further discloses a dual mode processor having at least two operational modes including a first high performance mode and a second low power mode in column 1, lines 65-68, column 2, lines 1-14 and 59-68 and column 3, lines 42-68, wherein when the system is acting as only an 8 bit system, only an 8 bit processor is powered, therefore allowing 8 bit mode to consume less power than 16 bit mode. Additionally, Berger discloses logic equipped to selectively provide the dual mode processor with the first or second operating system in response to the operational mode of the dual mode processor in column 2, lines 2-28.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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DiNicola (U.S. Patent No. 5,394,524) discloses a multiple processor system with a switch between processors.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher J. Maier whose telephone number is (703) 605-1213. The examiner can normally be reached on Monday - Friday 8am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras can be reached on (703) 305-9720. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 703-9314 for regular communications and (703) 308-9051 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

Chris Maier


cjm
July 11, 2001


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